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HY51V17805B Series
2M × 8-bit CMOS DRAM with Burst EDO

DESCRIPTION

The HY51V17805B is the new generation and fast dynamic RAM organized 2,097,152x8-bit. The HY51V17805B utilized Hyundai's CMOS silicon gate process technology as well as advenced circuit techniques to prove wide operating margin to the users. This device can be packaged in industry-standard 28/28 plastic SOJ, TSOP-II and Reverse TSOP-II.

The HY51V17805B is a burst access DRAM in which all READ and WRITE cycles occur in bursts of four. The burst wrap around on a four byte boundary. This means only the two least significant bits of the $\overline{CAS}$ address are modified internally to produce each address of the burst sequence.

The burst type, interleave or linear, is determined by excuting a WCBR cycle with address A0 set to either HIGH or LOW. A0 LOW will program the device to excute linear bursts, A0 HIGH will program the bursts to be interleave. For future compatability it is strongly recommended that the information 0010 000X (where x=A0) is supplied on addresses A7-A0 during the WCBR cycle. The WCBR cycle must be followed by a $\overline{RAS}$-only or CBR refresh to exit programming mode.

FEATURES

- Low power dissipation
  Max. CMOS standby 0.83mW
  Max. TTL standby   0.33mW
  Max. operating

Speed	Power1	Power2
50	396mW	468mW
60	360mW	432mW
70	324mW	396mW

  NOTE
  Power1: Closed Row Burst Read/Write
  Power2: Open Row Burst Read/Write
- Single power supply of 3.3V±5%
- All inputs and outputs are LVTTL compatible with 5V input/out put tolerance
- Fast access and cycle time

Speed	tRAC	tCAC	tPC
50	52ns	10ns	15ns
60	60ns	11.6ns	16.6ns
70	70ns	15ns	20ns

- Burst EDO mode operation
- Multi-bit test capability
- Burt order, interleave or linear, programmed by excuting WCBR cycle after initialization
- Industry-stardard x 8 pinout and package
- CAS-before-RAS, RAS-only refresh capability
- 2048 refresh cycles /32ms
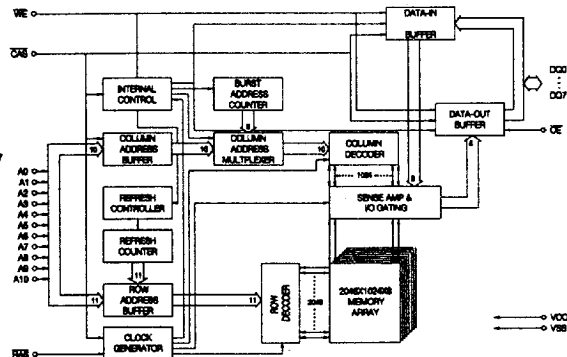- Four cycle EDO burst access

PIN DESCRIPTION

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
$\overline{OE}$	Output Enable
A0 - A10	Address Input
DQ0-DQ7	Data Input/Output
Vcc	Power (+3.3V)
Vss	Ground

PIN CONNECTION
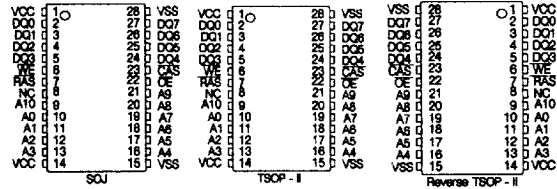
BLOCK DIAGRAM

■ 4675088 0004678 3T0 ■

EDO BURST MODE TRUTH TABLE

PRESENT-STATE	RESULTING STATE	RAS	CAS	WE	OE	ADDRESS		DATA
						Row	Column	DQ
Any	Idle	L → H	H	X	X	X	X	High-Z
Idle	Row Open	H → L	H	X	X	Row	X	High-Z
Idle	CBR REFRESH	H → L	L	H	X	X	X	High-Z
Row Open	RAS-only REFRESH	H→L→H	H	X	X	Row	X	High-Z
Row Open	READ burst	L	H→L	H	L	X	Col	Data-Out
Row Open	WRITE burst	L	H→L	L	X	X	Col	Data-In
READ burst	TERMINATE READ burst	L	H	H→L	X	X	X	High-Z
WRITE burst	TERMINATE WRITE burst	L	H	L→H	X	X	X	High-Z
Idle	PROGRAM burst type	H → L	L	L	X	A0[1]	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H → L	L	H	X	X	X	High-Z
PROGRAM	EXIT PROGRAM MODE	H→L→H	H	X	X	Row	X	High-Z

Note:
1. A WCBR cycle determines the burst sequence. A0=LOW sets burst sequence to linear, A0=HIGH set the burst sequence to interleave, A8 through A10 are don't care. A7-A0 should contain the sequence (0010 000X where X=A0) to ensure future compatability. A refresh cycle (RAS-only or CBR) must follow WCBR cycle to exit the programming mode.

INTERLEAVE BURST SEQUENCE TABLE

OPERATION	ADDRESSES USED		
	A9 - A2	A1	A0
First access, register external CAS address	A9 - A2	A1	A0
Second access (first burst address)	registered A9 - A2	registered A1	registered A̅0̅
Third access (second burst address)	registered A9 - A2	registered A̅1̅	registered A0
Fourth access (third burst address)	registered A9 - A2	registered A̅1̅	registered A̅0̅

INTERLEAVE BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X...X01	X...X10	X...X11
X...X01	X...X00	X...X11	X...X10
X...X10	X...X11	X...X00	X...X01
X...X11	X...X10	X...X01	X...X00

LINEAR BURST ADDRESS TABLE

FIRST ADDRESS	SECOND ADDRESS	THIRD ADDRESS	FOURTH ADDRESS
X...X00	X...X01	X...X10	X...X11
X...X01	X...X10	X...X11	X...X00
X...X10	X...X11	X...X00	X...X01
X...X11	X...X00	X...X01	X...X10

ABSOLUTE MAXIMUM RATING

SYMBOL	PARAMETER	RATING	UNIT
T_A	Ambient Temperature	0 to 70	°C
T_{STG}	Storage Temperature	-55 to 150	°C
V_{IN}, V_{OUT}	Voltage on Any Pin Relative to Vss	-0.1 to 5.5	V
I_{OS}	Short Circuit Output Current	50	mA
P_D	Power Dissipation	1.1	W

NOTE:Operation at or above Absolute Maximum Ratings can adversely affect device reliability.

RECOMMENDED DC OPERATING CONDITIONS

(T_A = 0°C to 70°C)

SYMBOL	PARAMETER	MIN.	MAX.	UNIT	NOTE
V_{CC}	Power Supply Voltage	3.13	3.47	V	
V_{IH}	Input High Voltage	2.0	5.5	V	2
V_{IL}	Input Low Voltage	-1.0	0.8	V	2

NOTE: All Voltage are referenced to Vss.

DC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V±5%, Vss=0V, unless otherwise noted.)

SYMBOL	PARAMETER	TEST CONDITIONS	SPEED/POWER	MIN.	MAX.	UNIT	NOTE
I_{LI}	Input Leakage Current (Any Input Pins)	$0V \leq V_{IN} \leq 5.5V$ All other pins not under test = 0V		-2	2	µA	
I_{LO}	Output Leakage Current (High impedance State)	$0V \leq V_{OUT} \leq 5.5V$ $\overline{RAS}$ & $\overline{CAS}$ at V_{IH}		-10	10	µA	
I_{CC1}	Vcc Supply Current, TTL Standby	$\overline{RAS}$ & $\overline{CAS}$ at V_{IH} (min.), other Inputs $\geq$ Vss		-	2	mA	
I_{CC2}	Vcc Supply Current, CMOS Standby	$\overline{RAS}$ & $\overline{CAS} \geq$ Vcc-0.2V		-	0.5	mA	
I_{CC3}	Vcc Supply Current, Operating ; Closed Row Burst Read / Write	$t_{PC} = t_{PC}$ (min): 50% duty cycle on $\overline{RAS}$: Open Row, 4 Cycle Burst, Close Row	50 60 70	- - -	110 100 90	mA	5
I_{CC4}	Vcc Supply Current, Operating : Open Row Burst Read / Write	$t_{PC} = t_{PC}$ (min): Alternating 4 cycles inactivity	50 60 70	- - -	130 120 110	mA	5
I_{CC5}	Vcc Supply Current, $\overline{RAS}$-only refresh	$t_{PC} = t_{PC}$ (min.)	50 60 70	- - -	150 140 130	mA	4
I_{CC6}	Vcc Supply Current, $\overline{CAS}$-before-$\overline{RAS}$ refresh	$t_{RC} = t_{RC}$ (min.)	50 60 70	- - -	150 140 130	mA	4,6
V_{OL}	Output Low Voltage	$I_{OL} = 2mA$		-	0.4	V	
V_{OH}	Output High Voltage	$I_{OH} = -2mA$		2.4	-	V	

CAPACITANCE

(TA=25°C, Vcc=3.3V±5%, Vss=0V, f=1MHz, unless otherwise noted.)

SYMBOL	PARAMETER	MIN	MAX	UNIT	NOTE
C_{I1}	Input Capacitance : Address		5	pF	3
C_{I2}	Input Capacitance : $\overline{RAS}$		6	pF	3
C_{I3}	Input Capacitance : $\overline{CAS}$, $\overline{WE}$, $\overline{OE}$		5	pF	3
C_{I0}	Data Input/Output Capacitance : DQ		7	pF	3

AC CHARACTERISTICS

(TA=0°C to 70°C, Vcc=3.3V ± 5%, Vss=0V, unless otherwise noted.) NOTE: 7, 8, 9, 10, 11

#	SYMBOL	PARAMETER	HY51V17805BJC/TC/RC						UNIT	NOTE
			-50		-60		-70			
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
1	tPC	Burst EDO Cycle Time	15	-	16.6	-	20	-	ns	
2	tRAC	Access Time from RAS	-	50	-	60	-	70	ns	
3	tCAC	Access Time from CAS	-	10	-	11.6	-	15	ns	
4	tAA	Access Time from Column-Address	-	25	-	28.2	-	35	ns	12
5	tOEA	Output Enable Access Time	-	10	-	12	-	15	ns	
6	tCOH	Data Hold Time from CAS Low	3	-	3	-	3	-	ns	
7	tRAS	RAS Pulse Width	50	125K	60	125K	70	125K	ns	
8	tRP	RAS Precharge Time	30	-	40	-	50	-	ns	
9	tRSH	RAS Hold Time	0	-	0	-	0	-	ns	
10	tCAS	CAS Pulse Width	5	10K	5	10K	5	10K	ns	
11	tCP	CAS Precharge Time	5	-	5	-	5	-	ns	
12	tRCD1	RAS to CAS Delay Time	20	-	16.6	-	20	-	ns	
13	tRCD2	RAS to CAS Delay Time	40	-	46.6	-	55	-	ns	
14	tCRP	CAS to RAS Precharge Time	10	-	10	-	10	-	ns	
15	tASR	Row-Address Set-up Time	1.5	-	1.5	-	1.5	-	ns	
16	tRAH	Row-Address Hold Time	8.5	-	8.5	-	8.5	-	ns	
17	tASC	Column-Address Set-Up Time	1.5	-	1.5	-	1.5	-	ns	
18	tCAH	Column-Address Hold Time	8.5	-	8.5	-	8.5	-	ns	
19	tRCS	Read Command Set-Up Time	3	-	4	-	5	-	ns	
20	tRCH	Read Command Hold Time	5	-	5	-	5	-	ns	
21	tOEP	OE High Pulse Width	10	-	10	-	10	-	ns	
22	tOELZ	OE to Output Low-Z	3	-	3	-	3	-	ns	13
23	tOD	Output Disable	4	10	4	10	4	15	ns	13
24	tOES	Output Enable Set-Up (Only near CAS)	3	-	3	-	3	-	ns	
25	tOEH	Output Enable Hold (Only near CAS)	5	-	5	-	5	-	ns	
26	tCLZ	CAS to Output in Low-Z	3	-	3	-	3	-	ns	13
27	tOFF	Output Buffer Turn-Off Delay	4	10	4	10	4	15	ns	13
28	tBTH	Burst Terminate Hold Time	3	-	3	-	3	-	ns	
29	tBTHZ	Output Disable From Burst Terminate	7	13	7	13	7	13	ns	13,16
30	tWCS	WE Command Set-Up Time	3	-	4	-	5	-	ns	
31	tWCH	Write Command Hold Time	5	-	5	-	5	-	ns	
32	tWHZ	WE to Output High-Z	4	10	4	10	4	15	ns	13,16
33	tTP	Burst Term Inate Pulse Width	6	-	6	-	8	-	ns	14
34	tCRW	CAS Low to RAS High (Required Only for WRITE cycle)	15	-	16.6	-	20	-	ns	
35	tDS	Data-in Set-Up Time	0	-	0	-	0	-	ns	
36	tDH	Data-in Hold Time	5	-	5	-	5	-	ns	
37	tT	Transition Time (rise or fall)	1.5	50	1.5	50	1.5	50	ns	
38	tREF	Refresh Period (2048 Cycle)	-	32	-	32	-	32	ms	
39	tRPC	RAS to CAS Precharge Time	5	-	5	-	5	-	ns	
40	tRC	Random Read or Write cycle Time	90	-	110	-	130	-	ns	
41	tWRP	WE Set-Up Time (CBR or WCBR)	10	-	10	-	10	-	ns	
42	tWRH	WE Hold Time (CBR or WCBR)	10	-	10	-	10	-	ns	
43	tCPN	CAS Precharge Time (CBR or WCBR)	10	-	10	-	10	-	ns	
44	tCSR	CAS Set-Up Time (CBR or WCBR)	10	-	10	-	10	-	ns	6
45	tCHR	CAS Hold Time (CBR or WCBR)	15	-	15	-	15	-	ns	6

NOTE:

1. All voltage referenced to Vss.
2. Input Power-up : VIH ≤ +5.5V and VCC ≤ +3.13V
   for t ≤ 200msec.
3. This parameter is sampled. VCC=3.3V ± 5% : f=1 MHz
4. Icc is dependent on cycle rates.
5. Icc is dependent on output loading and cycle rates. Specified values are obtained with minimum tPC and 50 percents duty cycle. The outputs are open.
6. Enables on-chip refresh and address counters.
7. Initialization consists of an initial pause of 100µs after power-up followed by eight $\overline{RAS}$ refresh cycles ($\overline{RAS}$-only or CBR with $\overline{WE}$ HIGH). This sequence must be executed before proper device operation is assured. The eight $\overline{RAS}$ cycle wake-ups should be repeated any time the tREF refresh requirement is exceeded. A WCBR cycle must be executed to initalize the burst type, interleave or linear followed by a $\overline{RAS}$-only or CBR refresh cycle.
8. AC characteristics assume tT=1.5ns.
9. All output timings are referenced to 1.5V and all input timings are referenced to 1.5V, unless otherwise specified. Inputs must be driven to the appropriate voltage levels indicated by the corresponding timing diagrams when A.C. specifications are measured, as shown in Figure 1.
10. In addition to meeting the transition rate specification, all input signals must transit between VIH and VIL (or between VIL and VIH) in a monotonic manner.
11. NC pins are assumed to be left floating and are not tested for leakage.
12. tAA is a calculated specification which is the sum of tPC and tCAC.
13. Output loading is specified with CL=5pF as Figure 2. Transition is measured ± 200mV from steady state voltage. These parameters are sampled.
14. Applies only during burst termination operation.
15. AC output loading is specified with CL=50pF as in Figure 3. Figure 4. is shown for reference. Transition is measured at the 1.5V referenced level.
16. The latter of tWHZ or tBTHZ satisfied will place the DQ pins in the High-Z state.
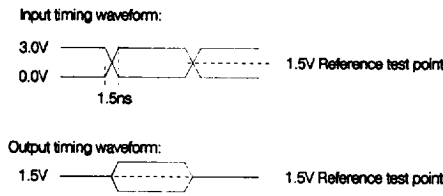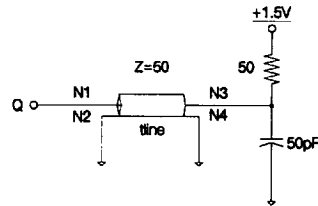

Fig. 1 TIMING SPECIFICATIONS
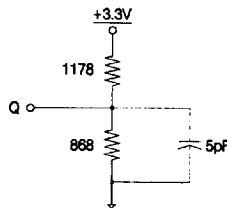
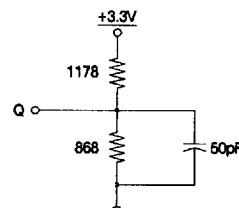Fig. 3 AC TIMING OUTPUT LOAD EQUIVALENT
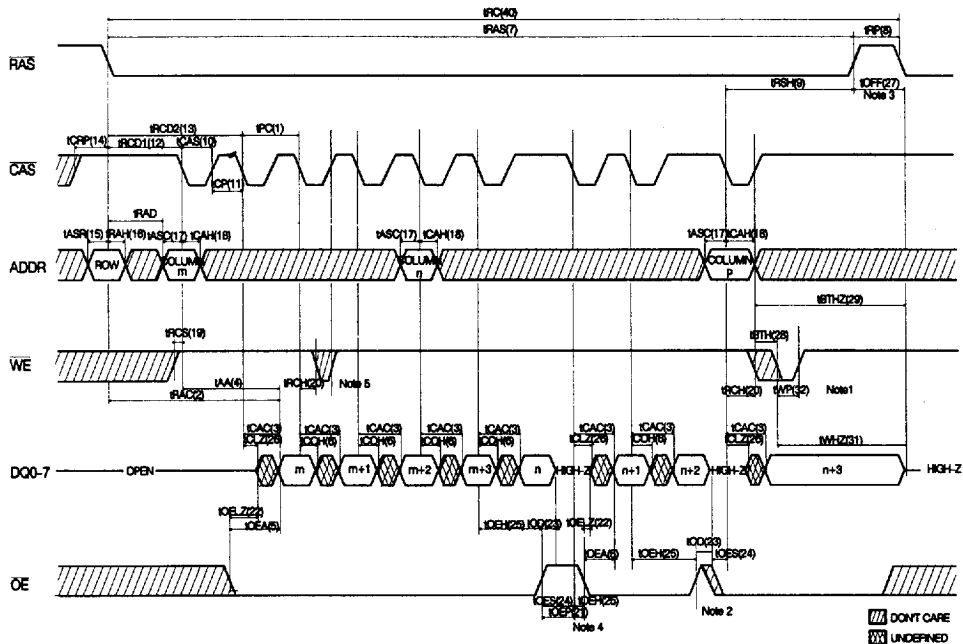
Fig. 2 HIGH-Z OUTPUT LOAD
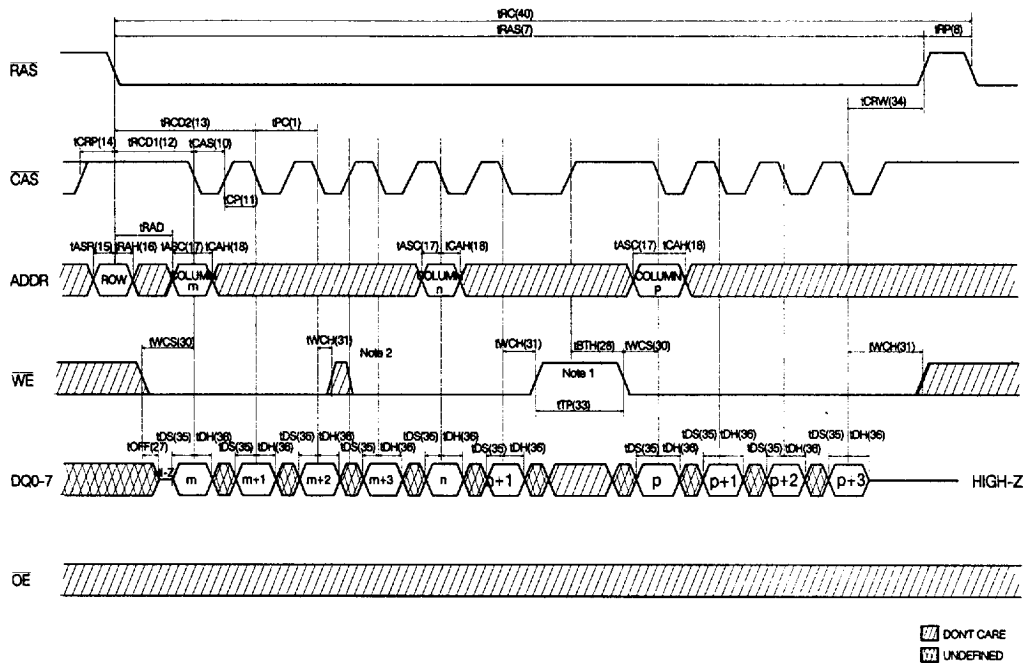
Fig. 4 OUTPUT LOAD EQUIVALENT

TIMING DIAGRAM

BURST EDO READ CYCLE

NOTE:

1. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided tTP and tBTH are satisfied. The DQs will be placed in the High-Z state once the latter of tWHZ or tBTHZ is satisfied.
2. When $\overline{CAS}$ is HIGH if $\overline{OE}$ transition HIGH during a burst READ cycle then transitions LOW, the outputs will remain in HIGH-Z until tCLZ after the next falling edge of $\overline{CAS}$.
3. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and tristate the bus. tOFF is measured from the last signal ($\overline{RAS}$ or $\overline{CAS}$) that transitions HIGH.
4. Output enable ($\overline{OE}$) is an asynchronous signal.
   The tOES and tOEH specifications are required only when Output enable transitions from active (LOW) to inactive (HIGH) either tOES, before the falling edge of $\overline{CAS}$ or tOEH, after the falling edge of $\overline{CAS}$.
   When $\overline{OE}$ transitions HIGH after $\overline{CAS}$ transitions LOW, the DQ pins are placed in the High-Z state and will remain in the High-Z state until another $\overline{CAS}$ LOW transitions occurs, regardless of the state of $\overline{OE}$.
5. $\overline{WE}$ transitioning LOW and returning HIGH prior to $\overline{CAS}$ going HIGH will not terminate the burst.
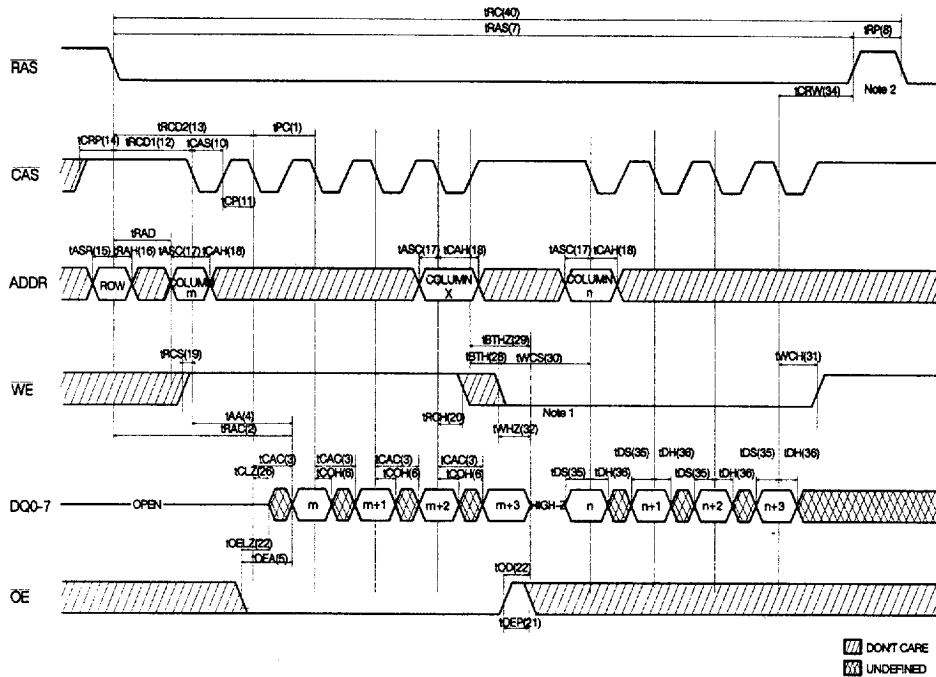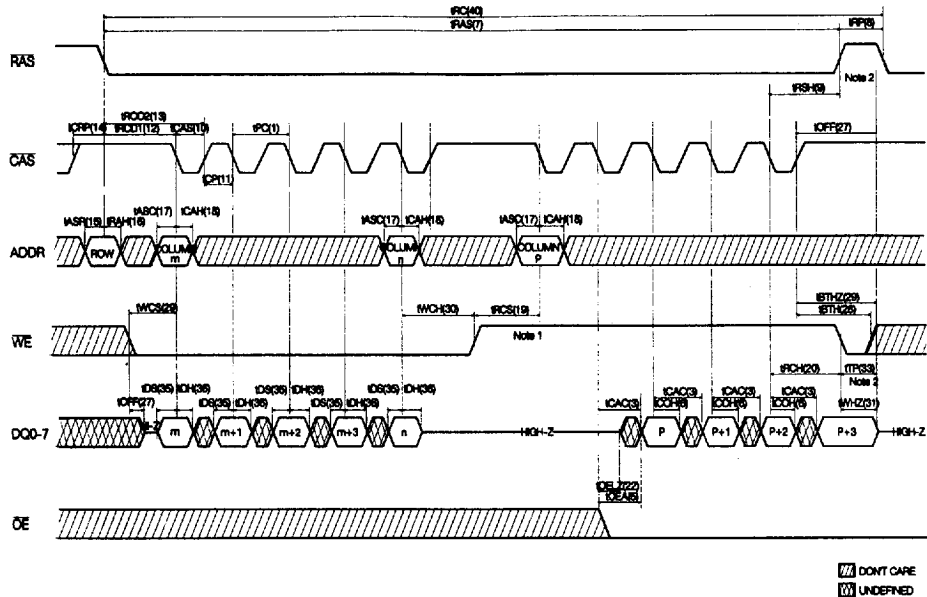
BURST EDO WRITE CYCLE

NOTE:

1. $\overline{\text{WE}}$ transitioning HIGH will terminate the burst and reset the burst counter provied tTP and tBTH are satisfied.
2. $\overline{\text{WE}}$ transitioning HIGH and returning LOW prior to $\overline{\text{CAS}}$ going HIGH will not terminate the burst.

BURST EDO READ / WRITE CYCLE

NOTE:

1. $\overline{WE}$ transitioning LOW will terminate the burst and reset the burst counter provided tTP and tBTH are satisfied. tTP is met by the READ burst being terminated by a WRITE burst. The DQs will be placed in the High-Z state once the latter of the tWHZ or tBTHZ is satisfied.
2. The combination of $\overline{RAS}$ and $\overline{CAS}$ HIGH close the row and place the DQs pins in the High-Z state.

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BURST EDO WRITE / READ CYCLE

NOTE:

1. WE transitioning HIGH will terminate the burst and reset the burst counter. The tBTH time is not required as it is satisfied by tRCS : tTP is met by the WRITE burst being terminated by a READ burst.
2. WE transitioning LOW will terminate the burst and reset the burst counter provided tTP and tBTH are satisfied. The DQs will be placed in the High-Z state once the latter of tWHZ or tBTHZ is satisfied.
3. The combination of RAS and CAS HIGH close the row and place the DQ pins in the High-Z state. tOFF is measured from the last signal (RAS or CAS) that transitions HIGH.

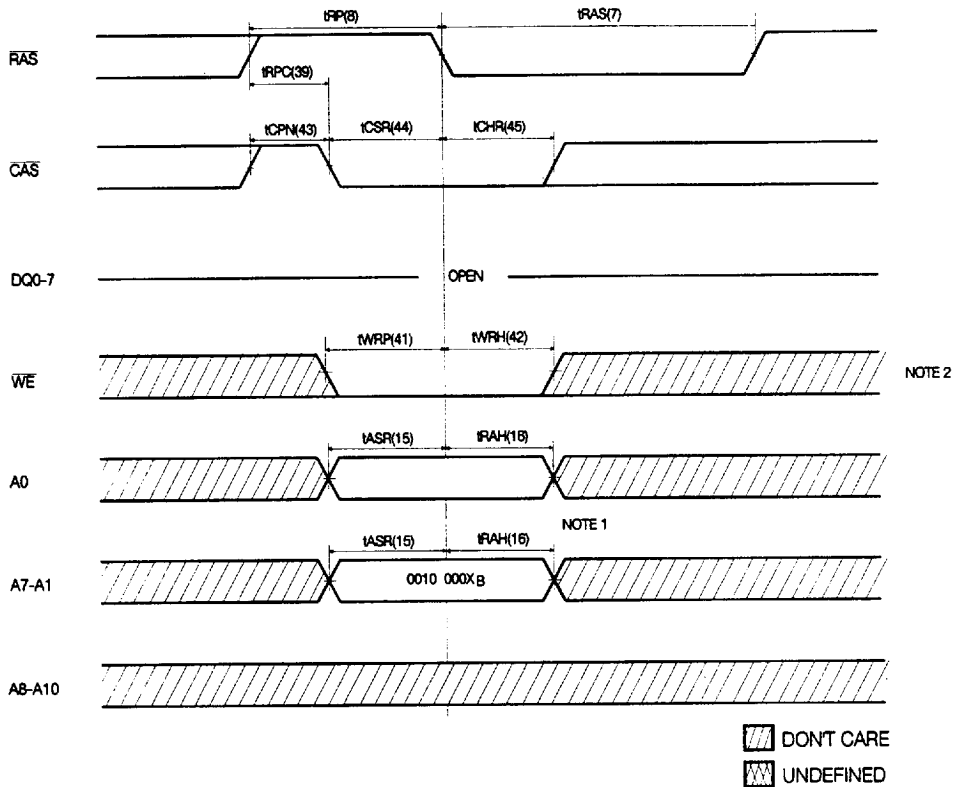## $\overline{RAS}$-ONLY REFRESH CYCLE

CBR REFRESH CYCLE

DON'T CARE
UNDEFINED

•¤YUNDAI
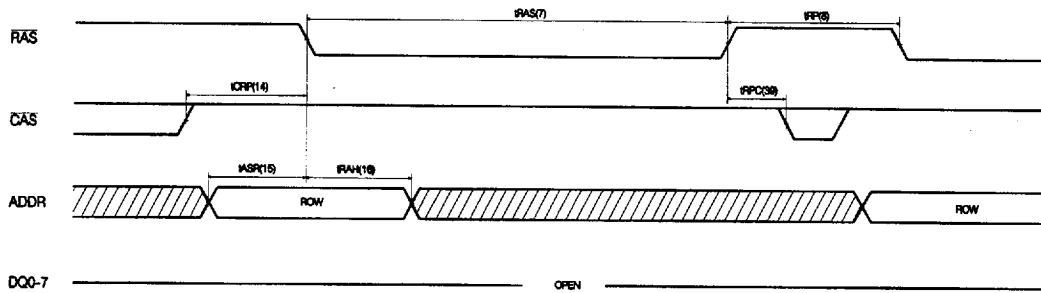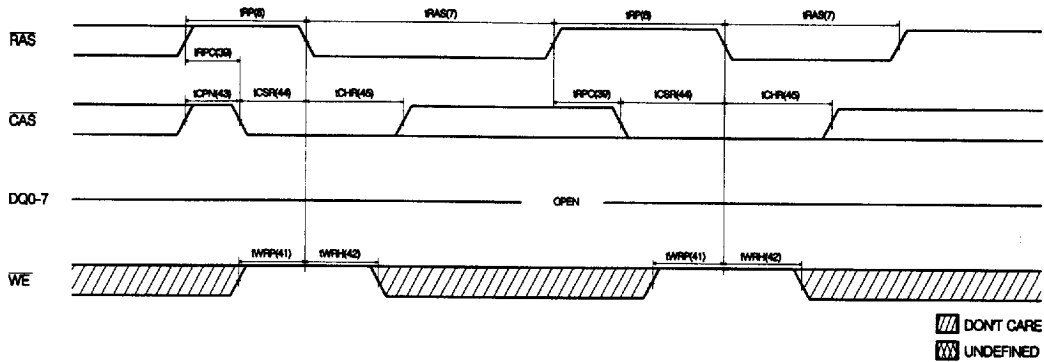
WCBR PROGRAM CYCLE

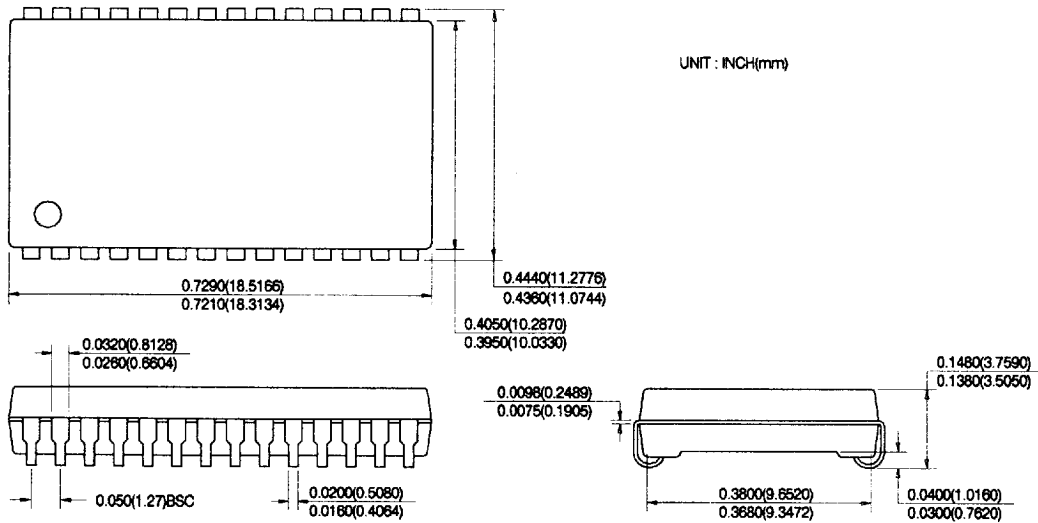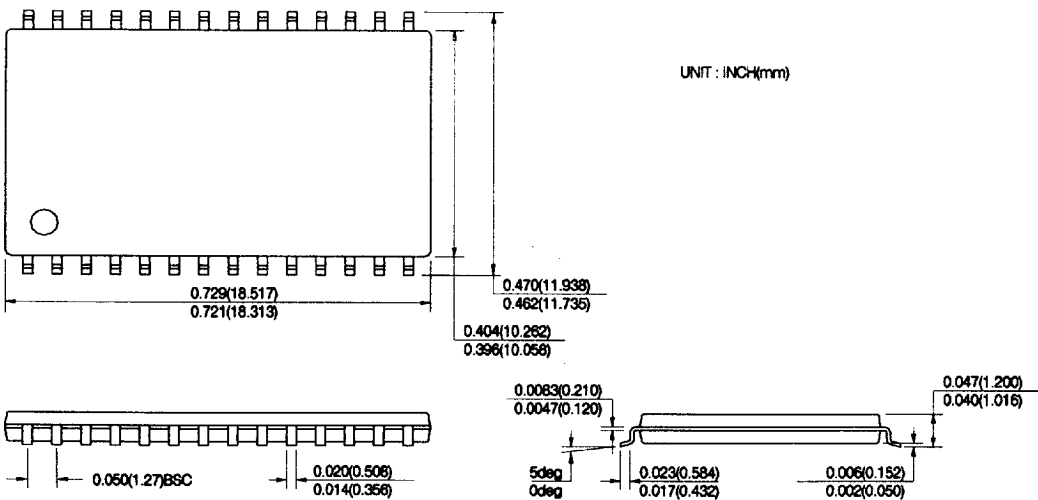|	
▨	DON'T CARE
▨	UNDEFINED

NOTE:

1. A0 LOW sets the burst sequence to linear bursts. A0 HIGH sets the burst sequence to interleave bursts. Addresses A8 through A10 are don't cares. Address A7-A1 should contain the state of (0010 000X$_B$ where x=A0) to ensure future compatability. The burst sequence will remain set until the device power is interrupted or another WCBR cycle is executed.
2. A $\overline{RAS}$-only or CBR refresh cycle must be executed after the WCBR cycle to exit the programming mode.

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PACKAGE INFORMATION

300 mil 28 pin Small Outline J-form Package (JC)

UNIT : INCH(mm)

0.7290(18.5166)
0.7210(18.3134)

0.4440(11.2776)
0.4360(11.0744)

0.4050(10.2870)
0.3950(10.0330)

0.0320(0.8128)
0.0260(0.6604)

0.0098(0.2489)
0.0075(0.1905)

0.1480(3.7590)
0.1380(3.5050)

0.050(1.27)BSC

0.0200(0.5080)
0.0160(0.4064)

0.3800(9.6520)
0.3680(9.3472)

0.0400(1.0160)
0.0300(0.7620)

300 mil 28 pin Thin Small Outline Package (TC) (RC)

UNIT : INCH(mm)

0.729(18.517)
0.721(18.313)

0.470(11.938)
0.462(11.735)

0.404(10.262)
0.396(10.058)

0.0083(0.210)
0.0047(0.120)

0.047(1.200)
0.040(1.016)

0.050(1.27)BSC

0.020(0.508)
0.014(0.356)

5deg
0deg

0.023(0.584)
0.017(0.432)

0.006(0.152)
0.002(0.050)

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ORDERING INFORMATION

PART NO	SPEED	POWER	PACKAGE
HY51V17805BJC	50/60/70		SOJ
HY51V17805BTC	50/60/70		TSOP-II
HY51V17805BRC	50/60/70		TSOP-II(R)

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